Product Line

Verification Ecosystem for FPGA/SoC Designs

A trusted name in EDA since 1984, Aldec understands that today's engineers require innovative solutions to enable rapid deployment at every stage of development.

Aldec works closely with customers to understand their real-world challenges and requirements, and deliver a personal blueprint of solutions customized to fit their needs. High-Performance Simulator for Mixed Language Designs
IEEE VHDL, SystemVerilog, Verilog-AMS, SystemC/C/C++
Verification Libraries: UVM, OS-VVM
Assertion-Based Verification: SVA. PSJ.

Riviera-PRO™

ADVANCED VERIFICATION

FPGA DESIGN

IEEE VHDL, Verilog, SystemVerilog (Design) Multi-FPGA & EDA Tool Design Flow Manager HTML and PDF Design Documentation Text, Schematic, FSM Design Entry Tools

Active-HDL™

HES-DVM™ & SIMULATION

HES-7™

ARM® Cortex®-A9 Support with Xilinx® Zvng® SoC

HDMI, USB, Bluetooth, Wi-Fi, Ethernet, and more

Expandable, Non-proprietary Connectors

Scalable up to 144 million ASIC gates

Acceleration, SCE-MI Emulation, Prototyping
Virtual Platform Integration – HW/SW Co-Verification
Transactor Library - Bus Models and Peripherals
Extensive Debugging Capabilities

HW/SW EMULATION DESIGN RULE CHECKING

PROTOTYPING BOARDS

> HIGH-LEVEL SYNTHESIS

REQUIREMENTS

LIFECYCLE

MANAGEMENT

FPGA LEVEL IN-TARGET TESTING

MICROSEMI™ RAD-TOLERANT PROTOTYPING

ALINTTM

Industry-leading Rule Libraries: STARC, RMM, DO-254
Early Bug Detection during RTL Design Phase
IEEE VHDL, Verilog, Mixed-Language Designs
IDE for In-Depth Design Troubleshooting

/CyberWorkBench®

Supports control dominated circuits, datapath module Dedicated support for Altera® & Xilinx® FPGAs Automatic pipelining, Power optimization C-based Formal Verification (Assertions, Properties)

Spec-TRACER™

Traceability to HDL Design and Testbench

Requirements Coverage Analysis

Change Impact Analysis Test-Results Management

Supported Microsemi Devices/Capacities RTAX-S/SL Up To 4000S, RTAX-DSP & RTSX-SU Device Automated Device Netlist Converter Memory & Physical Design Constraint (PDC) File Conversion

RTAX/RTSX

DO-254/CTS™

Increase verification coverage by test
Testbench reuse as hardware test vectors
100% device I/O controllability and visibility
Testing at-speed on target device:
Altera®, Microsemi®, Xilinx®





Customer Stories

Active-HDL™



"With a good editor/compiler and a versatile, easy to use simulator, Active-HDL was considered the best featured design tool compared to leading competitors. The quality of the design environment and good integration with source control tools definitely saves time on both new development and maintaining existing code."

DO-254/CTS™

THALES

"Our project involved an Altera® Cyclone® II FPGA with multiple clocks and speeds in excess of 128 MHz. We wanted a complete verification path with requirements traceability and simulation results maintenance to validate that our system would work on the final hardware we deliver to our customer. Aldec's DO-254/ED-80 CTS gave us an effective way to meet the Level B Verification process requirements imposed by the DO-254 certification authorities."

Technical Support



"Thanks to Aldec's support team, learning how to simulate a new and rather complex design took nearly no time at all. It is quite clear that Aldec's engineers have left no stone unturned in their quest for excellence."

Riviera-PRO™



"Riviera-PRO provided Infineta with high speed simulation of high-density Verilog design with DPI connections for system software integration. Riviera-PRO is used by individual engineers for interactive debugging and regressions on an automated, multi-node simulator farm."

ALINT™



"Prior to using ALINT from Aldec, all VHDL code had to be personally reviewed by a principal engineer. This was becoming an increasingly laborious task consuming large amounts of valuable time and had the potential to miss errors – especially in larger projects. Using ALINT means that code can be checked by a design engineer much earlier in the design cycle, thus increasing effectiveness and reducing development time by reducing code errors. The final review can now rely on the ALINT reports – simplifying the process, thus reducing the time taken for approval."

Microsemi® RTAX Prototyping



"We had a very aggressive schedule. We needed a way to quickly verify the design functionality and integrate support. The Aldec prototyping adaptor saved us two months off our development schedule and over \$72,000 off our project costs."

