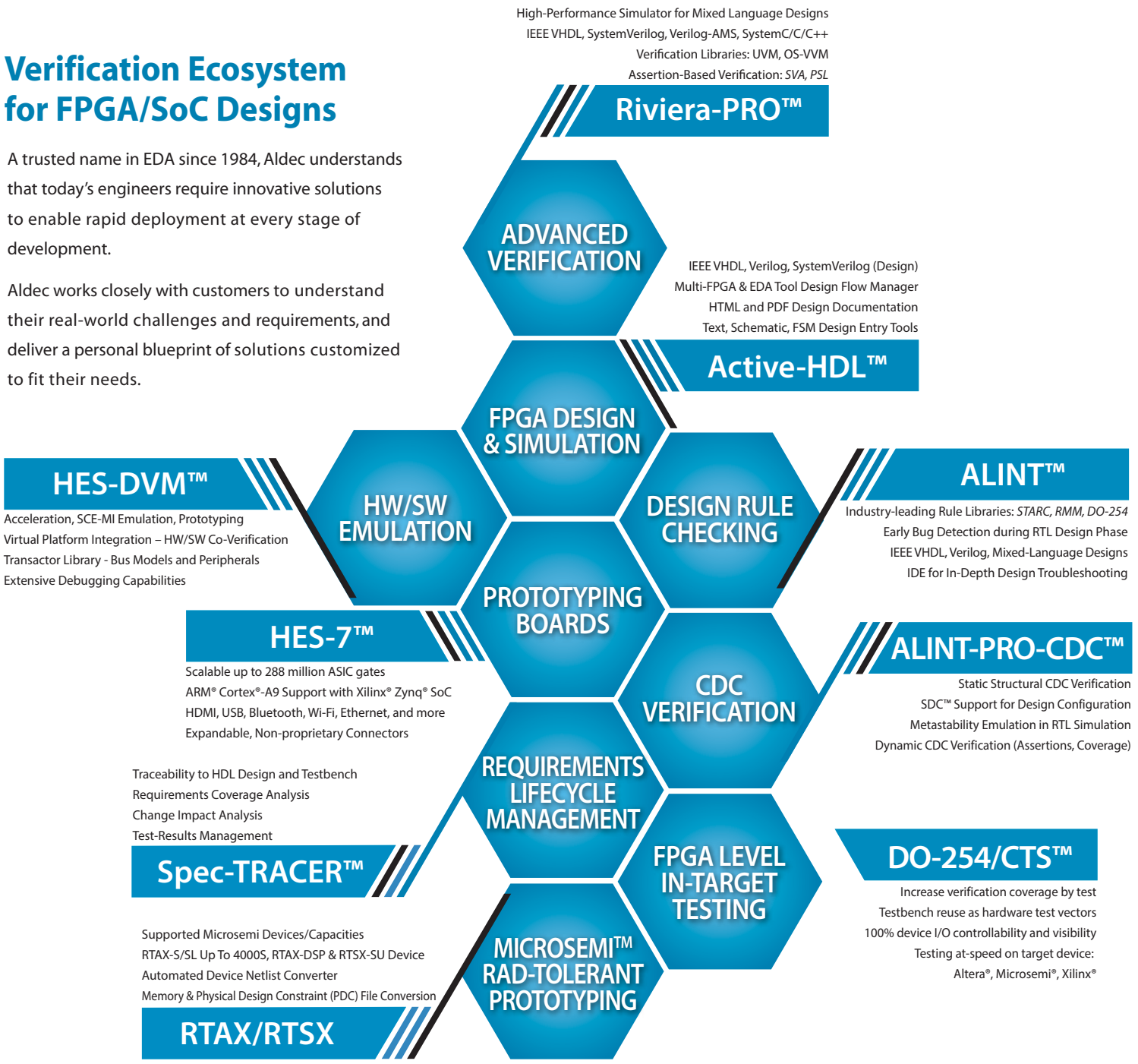
Product Line

Verification Ecosystem for FPGA/SoC Designs

A trusted name in EDA since 1984, Aldec understands that today's engineers require innovative solutions to enable rapid deployment at every stage of development.

Aldec works closely with customers to understand their real-world challenges and requirements, and deliver a personal blueprint of solutions customized to fit their needs.



High-Performance Simulator for Mixed Language Designs
IEEE VHDL, SystemVerilog, Verilog-AMS, SystemC/C/C++
Verification Libraries: UVM, OS-VVM
Assertion-Based Verification: *SVA, PSL*

Riviera-PRO™

IEEE VHDL, Verilog, SystemVerilog (Design)
Multi-FPGA & EDA Tool Design Flow Manager
HTML and PDF Design Documentation
Text, Schematic, FSM Design Entry Tools

Active-HDL™

HES-DVM™

Acceleration, SCE-MI Emulation, Prototyping
Virtual Platform Integration – HW/SW Co-Verification
Transactor Library - Bus Models and Peripherals
Extensive Debugging Capabilities

ALINT™

Industry-leading Rule Libraries: *STARC, RMM, DO-254*
Early Bug Detection during RTL Design Phase
IEEE VHDL, Verilog, Mixed-Language Designs
IDE for In-Depth Design Troubleshooting

HES-7™

Scalable up to 288 million ASIC gates
ARM® Cortex®-A9 Support with Xilinx® Zynq® SoC
HDMI, USB, Bluetooth, Wi-Fi, Ethernet, and more
Expandable, Non-proprietary Connectors

ALINT-PRO-CDC™

Static Structural CDC Verification
SDC™ Support for Design Configuration
Metastability Emulation in RTL Simulation
Dynamic CDC Verification (Assertions, Coverage)

Traceability to HDL Design and Testbench
Requirements Coverage Analysis
Change Impact Analysis
Test-Results Management

Spec-TRACER™

DO-254/CTS™

Increase verification coverage by test
Testbench reuse as hardware test vectors
100% device I/O controllability and visibility
Testing at-speed on target device:
Altera®, Microsemi®, Xilinx®

Supported Microsemi Devices/Capacities
RTAX-S/SL Up To 4000S, RTAX-DSP & RTSX-SU Device
Automated Device Netlist Converter
Memory & Physical Design Constraint (PDC) File Conversion

RTAX/RTSX

Customer Stories

Active-HDL™

"With a good editor/compiler and a versatile, easy to use simulator, Active-HDL was considered the best featured design tool compared to leading competitors. The quality of the design environment and good integration with source control tools definitely saves time on both new development and maintaining existing code."

Riviera-PRO™

"Designers seeking superb verification tools will benefit from Riviera-PRO's complete verification environment for high-performance RTL and gate-level simulation."

DO-254/CTS™

EASA approved our verification process based on Aldec DO-254/CTS, accepted our test results, and the audit passed without any findings. This is the first time in Elbit's history that we have been able to bring more than 5 FPGA devices to the audit. Aldec helped us solve several of our verification challenges and delivered quick and professional responses for all our requests.

Technical Support

"Thanks to Aldec's support team, learning how to simulate a new and rather complex design took nearly no time at all. It is quite clear that Aldec's engineers have left no stone unturned in their quest for excellence."

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ALDEC®
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