AL8051 Core
Application Note

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General Information

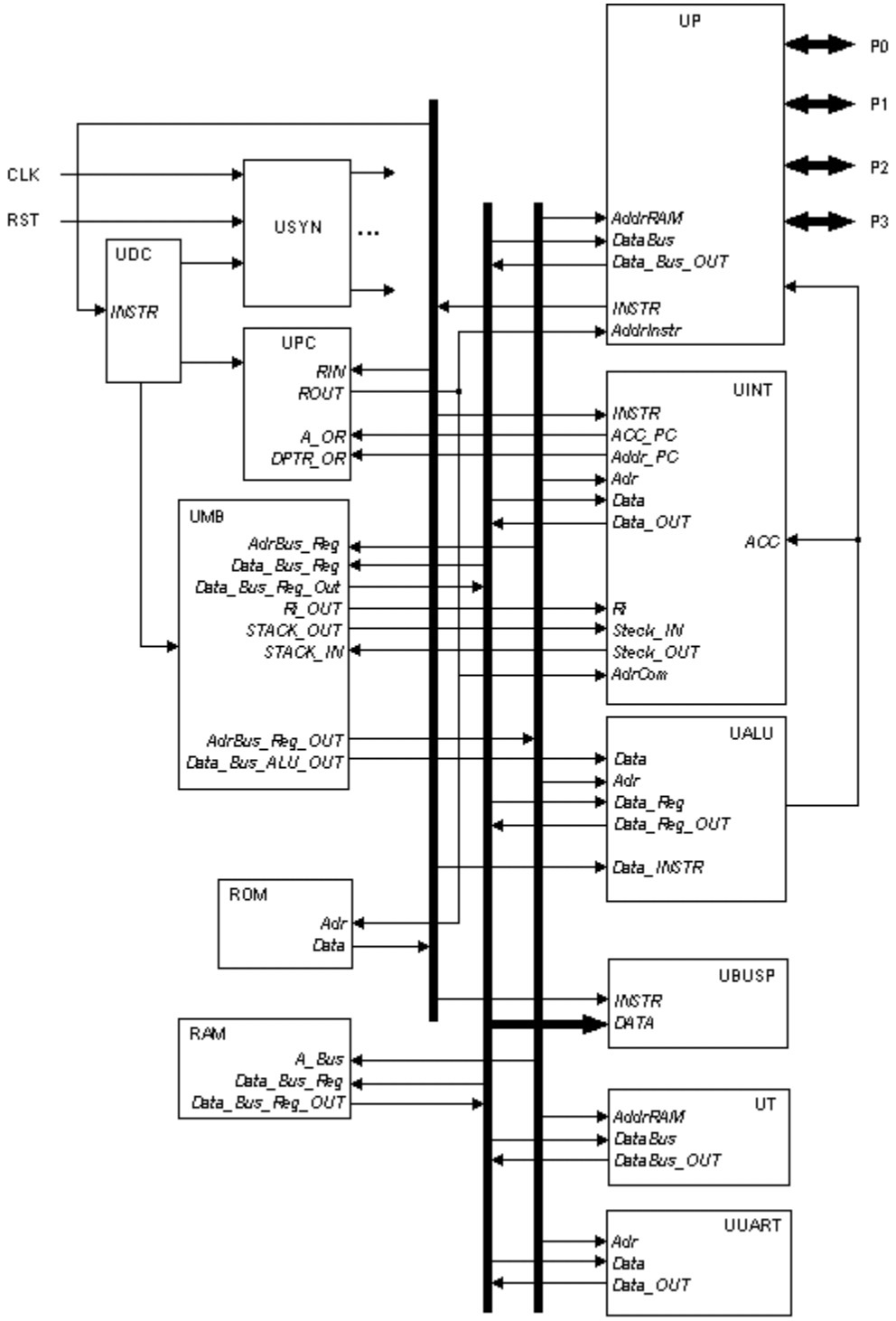
The AL8051 core is the VHDL model of the Intel™ 8-bit 8051 micro controller. The model is fully compatible with the Intel 8051 standard.

Features

- Opcode and Cycle Equivalent to Intel standard 8051
- Up to 8K Bytes Internal Program Memory (ROM)
- Up to 256 Bytes Internal Data Memory (RAM)
- Up to 64K Bytes External Program Memory address space
- Up to 64K Bytes External Data Memory address space
- Up to 128 Special Function Registers (SFR)
- 32 bidirectional and individually addressable I/O Lines
- Two 16-bit timer/counters
- Third timer/counter (optional)
- Full Duplex UART (Serial Port)
- 6-Source/5-Vector Interrupt Structure with Two Priority Levels

Block Diagram

The basic structure of the AL8051 core is shown below:



Contents

A. RTL soft macro code (VHDL or Verilog)

See the Deliverables section of this document for further details.

B. Test Vectors

See the Deliverables section of this document for further details.

Interface

The pinout of the AL8051 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the table.

Signal Name	Signal Direction	Polarity	Description
CLK [1)]	IN	-	Clock input
EA [2)]	IN	LOW	External Access
RST [2)]	IN	HIGH	Synchronous reset
ALE [2)]	OUT	HIGH	Address Latch Enable
PSEN [2)]	OUT	LOW	Program Store Enable
P0[7:0] [3)]	INOUT	-	Port P0
P1[7:0] [3)]	INOUT	-	Port P1
P2[7:0] [3)]	INOUT	-	Port P2
P3[7:0] [3)]	INOUT	-	Port P3

NOTES:

1. XTAL1 and XTAL2 original device pins were replaced with one CLK (clock) input signal. The clock frequency value has no limitations during the functional simulation.

2. EA, RST, ALE and PSEN signals behave exactly the same as the original device and are compatible with the Intel 8051 standard.

3. In the synthesizable model, each bidirectional pin is defined in the core interface as two separated VHDL ports. Optionally, using the AL8051 VHDL Interface (See the Deliverables section of this document for further details), it can be merged to one bidirectional port.

Implementation Data

The core has been synthesized and implemented to different types of reprogrammable devices. The model has been verified using the simulation environment and tested on the real hardware.

Software				
Synthesis Tool	Synopsys FPGA Express™ build 2.1.3.3220			
Implementation Tools	Xilinx Foundation™ 2.1i SP2, Altera MAX+plusII™ 9.21, Quartus™ 1.0 A			
Verification Tool	Active-HDL™ 5.1			
Hardware				
Vendor	Xilinx		Altera	
Device Family	4K	Virtex™	FLEX™ 10K	APEX™ 20K
Target Device	XC4062XLA-9	XCV300-4	EPF10K100-1	APEX20
Area*)	850CLBs (37%)	1064Slices (34%)	2201LCs (44%)	soon come
System Clock fmax	25MHz	26MHz	18MHz	soon come

*) without ROM implemented

Deliverables

After you request the desired compiled synthesizable core, Aldec delivers the following files:

- Both technology-dependent EDIF (AL8051_CORE.EDN) and VHDL (AL8051_CORE.VHD) netlists
- AL8051 VHDL Interface (AL8051.VHD)
- Customizable internal program memory (ROMBLOCK.VHD)
- ROM GENERATOR tool
- RAM memory (SYNMEM128.NGC)
- Datasheet and Application Note
- Sample designs

Usually Aldec delivers both EDIF and VHDL netlists for customers who order the synthesizable model. The EDIF netlist is used for the place and route process and VHDL is the post-synthesis netlist used for the simulation only. Of course, both netlists are technology-dependent, because they are created after the synthesis where the customer needs to specify a vendor, target family, etc.

Aldec provides AL8051 VHDL Interface for its AL8051 core, which allows you to:

- use bidirectional pins for the core which normally has bidirectional ports splitted into two separated signals: IN and OUT
- use user-customized AL8051 internal program memory (ROM)
- use the Reset on Configuration (ROC) component

Aldec can provide also a set of VHDL test benches for their cores. Usually they are sold at the additional charge.

Source codes are sold on a case-by-case basis.